REMARKS

Claims 1, 3, 5-17 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,566,171 to Levinson. Claims 2, 4, and 31-36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Levinson in view of U.S. Patent No. 6,327,175 to Manapat et al. Claims 18-30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Levinson in view of U.S. Patent No. 4,674,082 to Flanagin et al.

Claim Rejections, 35 U.S.C. § 102

With regard to claim 1, Applicants respectfully maintain that Levinson fails to teach

> a plurality of pipeline stages for transmitting data across the network, each pipeline stage consuming a predetermined time period, thereby providing for a predetermined time period for transmission for each packet successfully sent between one of the initiator nodes and one of the target nodes.

The Office Action relies on the Abstract and col. 36-47 of Levinson to supply this teaching. The Abstract of Levinson teaches "a switching apparatus having a plurality of transceivers for interfacing directly with a like plurality of user nodes. Each of the transceivers having a receive and transmit through port for passing data to and from user nodes and a network." The plurality of transceivers fails to teach the plurality of pipeline stages recited in claim 1. The plurality of transceivers increases throughput by duplicating resources, not by the technique of pipelining. The pipelining technique according to an embodiment of the present invention is described in the Application, beginning at page 26, line 20, as breaking the execution of an operation "into several steps also called pipeline stages. Overlapped execution is achieved in that each stage operates on a different operation." In contrast, each of the transceivers of Levinson perform the same operation for each node.

Levinson does not include col. 36-47, but the Office Action apparently relies on col. 17, lines 36-47, because this section is later recited by the Office Action in reference to claim 31.

This portion of Levinson teaches that the long delay between the generation of a queued request and the transmission of that request to the switch matrix may be set to 'x' milliseconds. The delay reflects the average amount of time required to process a queued switch request. This time period is not associated with pipeline stages, thus failing to teach the predetermined time period consumed by each pipeline stage recited by claim 1.

At col. 11, lines 3-11, Levinson teaches that a switch apparatus may use "a pipelined deserializer having pipelined request registers that store both source and target node IDs for each connection request." However, the deserializer of Levinson works in combination with the serializer to function like a transceiver for the control electronics and control information (see Levinson, beginning at col. 5, line 33, and Figure 4). The control information is merely sent to and from the switching apparatus, which includes the control apparatus, not across the network (i.e., between one of the initiator nodes and one of the target nodes), as recited in claim 1. In addition, Levinson fails to teach the timing of the pipelining, whereas claim 1 recites a predetermined time period consumed by each pipeline stage. Therefore, Levinson fails to teach a plurality of pipeline stages for transmitting data across the network, each pipeline stage consuming a predetermined time period, thereby providing for a predetermined time period for transmission for each packet successfully sent between one of the initiator nodes and one of the target nodes, as recited in claim 1.

Accordingly, Applicants respectfully request that the rejection of claim 1 and all claims dependent thereon be reconsidered and withdrawn.

Claim Rejections, 35 U.S.C. § 103

With regard to claim 31, Applicants respectfully maintain that Levinson, alone or in combination with Manapat, fails to teach or suggest

> a synchronous pipelined switched network coupling the plurality of processing nodes, the pipelined network having a plurality of pipeline stages, the pipeline including at least an arbitration stage to obtain a path through the pipelined switched network, a

transfer stage transferring data over the path and an acknowledge stage, each stage being of equal length.

The Office Action relies on col. 5, lines 50-59 and col. 17, lines 36-47 of Levinson to supply this teaching. Beginning at col. 5, line 33, and with Reference to Figure 4, Levinson teaches switch matrix 106 and control electronics 116, which includes Interrupt Controller and Sequence Generator 410. The Office Action fails to point out how these sections of Levinson teach the pipeline stages, which include an arbitration stage, a transfer stage, and an acknowledge stage, as recited in claim 31.

The Office Action also relies on col. 17, lines 36-47. This portion of Levinson teaches that the long delay between the generation of a queued request and the transmission of that request to the switch matrix may be set to 'x' milliseconds. The delay reflects the average amount of time required to process a queued switch request. This time period is not associated with the length of pipeline stages, as recited by claim 31.

Manapat teaches a memory device that may be configured to operate in an asynchronous or synchronous mode (see Abstract), not a synchronous pipelined switched network, as stated in the Office Action. Although Manapat teaches pipeline stages for an output path in synchronous mode of a memory, Manapat fails to compensate for the deficiencies of Levinson by failing to teach or suggest a pipelined switched network. Therefore, Levinson, alone or in combination with Manapat fails to teach or suggest a synchronous pipelined switched network coupling the plurality of processing nodes, the pipelined network having a plurality of pipeline stages, the pipeline including at least an arbitration stage to obtain a path through the pipelined switched network, a transfer stage transferring data over the path and an acknowledge stage, each stage being of equal length, as recited by claim 31.

Accordingly, Applicants respectfully request that the rejection of claim 31 and all claims dependent thereon be reconsidered and withdrawn.

With regard to claim 18, Applicants respectfully maintain that Levinson, alone or in combination with Flanagin, fails to teach or suggest

> transmitting the information from an initiator node to a target node using a plurality of pipeline stages in the computer network, each pipeline stage having a fixed forwarding delay.

The Office Action relies on the Abstract and on col. 17, lines 36-47 of Levinson to supply this teaching. The Abstract of Levinson teaches "a switching apparatus having a plurality of transceivers for interfacing directly with a like plurality of user nodes. Each of the transceivers having a receive and transmit through port for passing data to and from user nodes and a network." The plurality of transceivers fails to teach the plurality of pipeline stages recited in claim 18. The plurality of transceivers increases throughput by duplicating resources, not by the technique of pipelining. The pipelining technique according to an embodiment of the present invention is described in the application, beginning at page 26, line 20, as breaking down the execution of an operation "into several steps also called pipeline stages. Overlapped execution is achieved in that each stage operates on a different operation." In contrast, each of the transceivers of Levinson perform the same operation for each node.

The Office Action also relies on col. 17, lines 36-47 of Levinson to teach the limitations of claim 18. This portion of Levinson teaches that the long delay between the generation of a queued request and the transmission of that request to the switch matrix may be set to 'x' milliseconds. The delay reflects the average amount of time required to process a queued switch request. This time period is not associated with pipeline stages, thus it fails to teach the predetermined time period consumed by each pipeline stage recited by claim 18.

Flanagin teaches "converting serial bit digital signals of a selected line rate from a plurality of sources into a single serial bit signal for time division multiplexing (TDM) in periodic frames by a central receiver" (see Abstract). The Office Action relies on Figures 10 and 11 and col. 5, lines 50-66 of Flanagin to teach

> overlapping an operation in one pipeline stage with another operation in another pipeline stage.

These portions of Flanagin teach the throughput of sixteen port cards divided into four information phases (see col. 5, lines 37-49). Each of these data are processed in one of the four quadrants of a sample interval. Although two of the bits in each packet overlap into adjacent quadrants, the overlapping START and ORDER WIRE bits "are stripped off of the serial data stream from each port card and presented directly to the I/O control circuitry. This eliminates the 'overlap' of the S and O bits between quadrants" (see col. 6, lines 15-19). The information scheduling of Flanagin teaches serially processing of data in time. In contrast, the pipelining technique of an embodiment of the present invention is described in the application, beginning at page 26, line 20, as breaking down the execution of an operation into several steps also called pipeline stages. Pipelined operations can be executed in parallel. Flanagin fails to teach pipeline stages, but instead teaches stripping data to avoid requiring a pipelined operation. Flanagin fails to teach overlapping an operation in one pipeline stage with another operation in another pipeline stage, as recited in claim 18 and fails to compensate for the deficiencies of Levinson by failing to teach or suggest a plurality of pipeline stages in a computer network, each pipeline stage having a fixed forwarding delay. Thus Levinson, alone or in combination with Flanagin, fails to teach or suggest the limitations recited in claim 18.

In view of the above amendments and remarks, Applicants respectfully submit that all claims are in condition for allowance and notice to that effect is respectfully requested. If there are any issues that the Examiner believes could be resolved via telephone conference, the Examiner is requested to contact the undersigned at the number indicated below.

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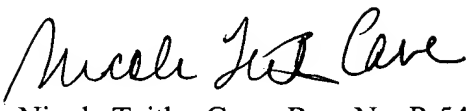

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